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Attorney's Docket N . 67,200-367 PATENT #9
10/29/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Weng Chang
Serial No.: 09/ 821,554
Filed: March 29, 2001
For: Dual Damascene Method Employing Composite Low Dielectric Constant Dielectric Layer Having Intrinsic Etch Stop Characteristics

Group Art Unit: 1765
Examiner: Lynette T. Umez Eronini

Assistant Commissioner for Patents
Washington, D.C. 20231

TRANSMITTAL OF APPEAL BRIEF (PATENT APPLICATION-37 CFR 192)

1. Transmitted herewith, in triplicate, is the APPEAL BRIEF in this application, with respect to the Notice of Appeal Filed on October 15, 2002 .

NOTE: "The Appellant shall, within 2 months from the date of the notice of appeal under §1.191(a) or within the time allowed for response to the action appealed from, if such time is later, file a brief in "triplicate", 37 C.F.R. 1.192(a) [emphasis added].

2. STATUS OF APPLICANT
This application is on behalf of:
X other than a small entity.
___ a small entity.

A verified statement:
___ is attached.
___ was already filed.

3. FEE FOR FILING APPEAL BRIEF
Pursuant to 37 CFR 1.17(f), the fee for filing the Appeal Brief is:
___ small entity $160.00
X other than a small entity $320.00

Appeal Brief fee due: $ 320.00

Certificate of Mailing/Transmission (37 CFR 1.8(a))

I hereby certify that this correspondence is, on the date shown below, being:

Mailing
X deposited with the U.S. Postal Service with sufficient postage as Express Mail Label No. EV 151 285 225 US in an envelope addressed to Box Appeal, Assistant Commissioner for Patents, Washington, D.C. 20231

Kathy Dixon

Dated: October 15, 2002

4. EXTENSION OF TERM

NOTE: The time periods set forth in 37 CFR 1.192(a) are subject to the provision of ☐1.136 for patent applications. 37 CFR 1.191(d). See also Notice of November 5, 1985 (1060 O.G. 27).

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136 apply:

(complete (a) or (b), as applicable)

(a) ☐ Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

	Extension (months)	Fee for other than small entity	Fee for small entity
☐	one month	$ 110.00	$ 55.00
☐	two months	$ 390.00	$195.00
☐	three months	$ 930.00	$465.00
☐	four months	$1,470.00	$735.00

Fee: $_____

If an additional extension of time is required, please consider this a petition therefor.

(check and complete the next item, if applicable)

☐ An extension for _____ months has already been secured, and the fee paid therefor of $_____ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request: $_____

or

(b) ☐ Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

5. TOTAL FEE DUE

The total fee due is:

Appeal Brief Fee: $ 320.00
Extension fee (if any) $_____

TOTAL FEE DUE: $ 320.00

6. FEE PAYMENT

X Attached is a Credit Card Payment Form for the sum of $ 320.00
X Charge Visa Credit Card No. 4756 8461 9568 0263 the sum of $ 320.00 .
A duplicate copy of this transmittal is attached.

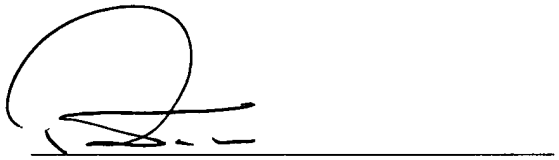
7. FEE DEFICIENCY

NOTE: If there is a fee deficiency and there is no authorization to charge an account, additional fees are necessary to cover the additional time consumed in making up the original deficiency. If the maximum six-month period has expired before the deficiency is noted and corrected, the application is held abandoned. In those instances where authorization to charge is included, processing delays are encountered in returning the papers to the PTO Finance Branch in order to apply these charges prior to action on the cases. Authorization to charge the deposit account for any fee deficiency should be checked. See the Notice of April 7, 1986, 1065 O.G. 31-33.

__X__ If any additional extension and/or fee is required, this is a request therefor to charge Visa Credit Card No. 4756 8461 9568 0263

And/Or

__X__ If any additional fee for claims is required, please charge Visa Credit Card No. 4756 8461 9568 0263



Signature of Attorney

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67,200-367
Serial Number 09/821,554

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES
APPEAL BRIEF

TO: Assistant Commissioner for Patents
Washington, D.C. 20231

FROM: Tung & Associates
838 West Long Lake Road - Suite 120
Bloomfield Hills, MI 48302

DATE: 4 October 2002

REF:

Applicant	:	Chang et al.	Filing Date	:	29 March 2001
Serial No..	:	09/821,554	Att'y No.	:	67,200-367; TSMC 00-407
Art Unit	:	1765	Examiner	:	Lynette T. Umez Eronini
Title	:	Dual Damascene Method Employing Composite Low Dielectric Constant Dielectric Layer Having Intrinsic Etch Stop Characteristics			

EXPRESS MAIL CERTIFICATE

"Express Mail" label number EV 151 285 225
Date of Deposit October 15, 2002

I hereby certify that this paper in triplicate and a credit card payment form in the amount of $320.00 (required filing fee) are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR §1.10 on the date indicated above and is addressed to: Box Appeal, Assistant Commissioner for Patents, Washington, D.C. 20231

Kathy Dixon

APPEAL BRIEF

Sir:

In response to rejection of the claims in the above referenced application for United States Patent in an office action mailed 7 August 2002 and made FINAL, applicant filed a notice of appeal on 15 October 2002. In accord with applicant's notice of appeal, please accept this appeal brief. No oral argument is requested.

1. Real Party in Interest

The real party in interest for this application is the assignee:

Taiwan Semiconductor Manufacturing Co., Ltd.
121 Park Avenue, No. 3
Science Based Industrial Park
Hsin-Chu, Taiwan, Republic of China

An assignment has been recorded for this United States Patent application.

2. Related Appeals and Interferences

There are no related appeals or interferences for this United States Patent application.

3. Status of the Claims

Claims 1-15 are pending in this application. Claims 1-15 are finally rejected under 35 U.S.C. § 103(a). Appeal is taken for claims 1-15 as finally rejected under 35 U.S.C. § 103(a).

4. Status of the Amendments

A response, filed 12 September 2002, was submitted in response to the office action made FINAL, in order to overcome the Examiner's rejections of the claims pending within this application. In an advisory action mailed on 19 September 2002, the Examiner indicated that

applicant's response was considered but did not place applicant's application in condition for allowance. The Examiner also indicated that applicant's response would be entered.

5. Summary of the Invention

The invention provides a dual damascene method for forming within a microelectronic fabrication a contiguous patterned conductor interconnect and patterned conductor stud layer within a corresponding trench contiguous with a corresponding via formed in turn formed through a dielectric layer formed of a comparatively low dielectric constant dielectric material, with enhanced microelectronic fabrication processing efficiency. (page 10, first full paragraph)

The invention realizes the foregoing object by employing when forming an aperture through a dielectric layer in accord with a dual damascene method and further in accord with the present invention, a composite dielectric layer comprising: (1) a patterned first dielectric layer formed of a first dielectric material having a first dielectric constant of less than about 4.0, the patterned first dielectric layer defining a via; and (2) a blanket second dielectric layer formed upon the patterned first dielectric layer and filling the via, the blanket second dielectric layer being formed of a second dielectric material having a second dielectric constant of less than about 4.0; where (3) the patterned first dielectric layer serves as an intrinsic etch stop within an anisotropic etch method employed for etching the blanket second dielectric layer to form therethrough an aperture comprising: (1) a trench; contiguous with (2) at least a portion of the via. (paragraph bridging pages 10-11)

The invention is claimed in two levels of scope including: (1) a method for forming an aperture through a dielectric layer (independent claim 1 and dependent claims 2-7); and (2) a derivative method for forming a patterned conductor layer within the aperture through the dielectric layer (independent claim 8 and dependent claims 9-15).

Independent claim 1 is read on the specification and drawings as follows:

1. A method for forming an aperture through a dielectric layer comprising:

providing a substrate 10 (Fig. 1; and page 14, second full paragraph);

forming upon the substrate 10 a patterned first dielectric layer 14a/14b/14c formed of a first dielectric material having a first dielectric constant of less than about 4.0, the patterned first dielectric layer 14a/14b/14c defining a via 15a/15b (Fig. 1; and page 17, first paragraph to page 19, first paragraph);

forming upon the patterned first dielectric layer 14a/14b/14c and filling the via 15a/15b a blanket second dielectric layer 16 formed of a second dielectric material having a second dielectric constant of less than about 4.0 (Fig. 1; and page 19, second paragraph to page 20, first full paragraph);

forming over the blanket second dielectric layer a patterned mask layer 18a/18b/18c which defines the location of a trench 19 to be formed through the blanket second dielectric layer 16, where an areal dimension of the trench is greater than and at least in part overlapping an areal dimension of the via 15a/15b (Fig. 1; and page 20, second full paragraph to page 21, first full paragraph); and

etching, while employing the patterned mask layer 18a/18b/18c in conjunction with an anisotropic etch method, the blanket second dielectric layer 16 to form an aperture 23a/23b comprising:

the trench 21a/21b; and

at least a portion of the via 15a/15b, where the patterned first dielectric layer 14a/14b/14c provides an intrinsic etch stop within the anisotropic etch method (Fig. 2; and page 22, first full paragraph to page 23, first full paragraph).

6. Issues

I. Whether claims 1-7 may properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Yu et al. (U.S. Patent No. 6,004,883; hereinafter "Yu") in view of Hopper et al. (U.S. Patent No. 6,030,901; hereinafter "Hopper") and Avanzino et al. (U.S. Patent No. 5,691,238; hereinafter "Avanzino").

II. Whether claims 8-15 may properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Yu in view of Hopper and Avanzino, and further in view of Chiang et al. (U.S. Patent No. 6,027,995; hereinafter "Chiang").

7. Grouping of Claims

Claims 1-7, group I, are directed towards a first claimed embodiment of the invention.

Claims 8-15, group II, are directed towards a second claimed embodiment of the invention.

The claims stand or fall together within their respective groups.

8. Argument

I. Claims 1-7 may not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Yu in view of Hopper and Avanzino.

II. Claims 8-15 may not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Yu in view of Hopper and Avanzino, and further in view of Chiang.

a. Yu Subject Matter

Yu (abstract and cover figure) discloses a dual damascene patterned conductor layer formation method without an etch stop layer. The method employs a patterned first dielectric layer formed of a first dielectric material which is not susceptible to etching within an oxygen containing plasma, in conjunction with a blanket second dielectric layer formed of a second dielectric material which is susceptible to etching within the oxygen containing plasma.

The Examiner cites Yu (paragraph 2, pages 2-3 of the office action made FINAL) as a base reference against which applicant's claims to applicant's invention are rejected.

b. Hopper Subject Matter

Hopper (abstract and cover figure) discloses a photoresist layer stripping method employing a hydrogen-nitrogen plasma such as to prevent an increase in dielectric constant of a low dielectric constant carbon containing dielectric material layer which is patterned while employing a photoresist layer which is desired to be stripped therefrom.

The Examiner cites Hopper (page 4, second paragraph of the office action made FINAL) as disclosing various carbon containing low dielectric constant dielectric materials

c. Avanzino Subject Matter

Avanzino (abstract and cover figure) discloses a subtractive dual damascene method which provides for forming an interconnection line having both upward and downward pointing stud layers.

The Examiner cites Avanzino (page 5, first paragraph of the office action made FINAL) as disclosing anisotropic etching within dual damascene processing.

d. Chiang Subject Matter

Chiang (abstract and cover figure) discloses a method for forming an interconnect structure which employs a hard mask layer and a low dielectric constant dielectric material.

The Examiner cites Chiang (page 6, first paragraph of the office action made FINAL) as disclosing chemical mechanical polish (CMP) planarizing methods for forming patterned conductor layers.

e. The Examiner's Assertions

At page 4, third paragraph of the office action made FINAL, the Examiner asserts that it would have been obvious to one of ordinary skill in the art at the time of the claimed invention to modify Yu by using a low dielectric constant dielectric material such as diamond like carbon as taught by Hopper, for the purpose of reducing parasitic capacitance between conductive patterns.

At page 5, second paragraph, of the office action made FINAL, the Examiner asserts that it would have been obvious to one of ordinary skill in the art at the time of applicant's invention by modifying Yu in view of Hopper by employing an anisotropic etch method as taught by Avanzino, for the purpose of controlling the shape of contact openings.

At page 6, second paragraph of the office action made FINAL, the Examiner asserts that it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to modify Yu in view of Hopper and Avanzino by employing a CMP

method for forming a patterned conductor stud layer within an aperture as taught by Chiang, for purposes of removing excess conductive material from the surface of a dielectric layer.

Within the continuation sheet, first full paragraph, of the advisory action, the Examiner asserts that applicant's claims do not require a laminated pair of dielectric layers.

Within the continuation sheet, last full paragraph, of the advisory action, the Examiner asserts that Hopper's dielectric materials would inherently provide an intrinsic etch stop within a dual damascene method.

f. Applicant's Responses

In response in a first instance, applicant asserts that none of applicant's claims to applicant's invention may properly be rejected under 35 U.S.C. § 103(a) over either of the above combinations of references insofar as: (1) Hopper, when viewed in its entirety, clearly teaches away from that which is disclosed and claimed by applicant within claim 1 and claim 8 and thus Hopper may not properly be employed in rejecting any of applicant's claims to applicant's invention under 35 U.S.C. § 103(a); and (2) none of the remaining references as cited by the Examiner provides, for purposes of rejecting applicant's claims to applicant's invention under 35 U.S.C. § 103(a), the limitations for which Hopper is cited.

With respect to Hopper, applicant in particular notes that while the Examiner accurately cites Hopper at col. 2, lines 47-55 as disclosing a multiplicity of low dielectric constant dielectric materials for forming patterned low dielectric constant dielectric layers which may define dual damascene apertures which may be filled employing dual damascene methods, Hopper's dual damascene structure as illustrated in Fig. 2 apparently illustrates with respect to a dual damascene aperture a patterned dielectric layer 22 formed of a single dielectric material rather than a laminated pair of dielectric material layers with intrinsic etch stop characteristics, as is required within applicant's invention as disclosed and claimed within claim 1 and claim 8. Thus, since applicant's dual damascene method as disclosed and claimed within claim 1 and claim 8 requires a laminated pair of dielectric material layers with intrinsic etch stop characteristics and Hopper discloses a dual damascene method clearly employing a single dielectric material layer 22 intrinsically, implicitly or inherently absent intrinsic etch stop characteristics, applicant asserts that Hopper in pertinent part, and when viewed in its entirely, teaches away from that which is disclosed and claimed by applicant. Thus, Hopper may not properly be employed in rejecting any of applicant's claims to applicant's invention under 35 U.S.C. § 103(a). MPEP 2141, 2141.02.

not req'd by claims

Since: (1) Hopper may not properly be employed in rejecting any of applicant's claims to applicant's invention under 35 U.S.C. § 103(a); and (2) none of the remaining prior art references as cited by the Examiner and employed in rejecting applicant's claims to applicant's invention alternatively provides the limitations for which Hopper was cited, applicant asserts that

none of applicant's claims to applicant's invention may properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over either: (1) Yu in view of Hopper and Avanzino; or (2) Yu in view of Hopper and Avanzino, and further in view of Chiang.

In response in a second instance, and as an alternative basis for traversing the Examiner's rejections of applicant's claims to applicant's invention under 35 U.S.C. § 103(a), applicant notes that all of the low dielectric constant materials disclosed by Hopper at col. 3, lines 47-55 are carbon containing low dielectric constant dielectric materials which Hopper within col. 2, last paragraph and col. 3, first two paragraphs discloses as each being seriously deteriorated or completely etched within an oxygen containing plasma. Since they are each deteriorated or etched within an oxygen containing plasma, applicant asserts that: (1) Hopper has not disclosed etch stop properties for any one of Hopper's low dielectric constant dielectric materials with respect to another of Hopper's low dielectric constant dielectric materials (i.e., each and every limitation within applicant's invention as disclosed and claimed within claim 1 and claim 8) (MPEP 2143, 2143.03); and (2) when substituted into Yu's invention in a fashion as suggested by the Examiner, a pair comprising two different of Hopper's low dielectric constant dielectric materials would presumably render Yu unsuitable for Yu's intended purpose since a dual damascene aperture would not be formed when etching a blanket second dielectric layer formed of a second of Hopper's low dielectric constant dielectric materials with respect to a patterned first dielectric layer formed of a first of Hopper's low dielectric constant dielectric materials (i.e, there is neither any suggestion or motivation to modify or combine Yu with Hopper nor is there any likelihood of success that the combination of Yu and Hopper will provide an operable invention) (MPEP 2143, 2143.01, 2143.02).

argues reason to combine

For these additional reasons, applicant asserts that: (1) applicant's claims 1-7 may not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Yu in view of Hopper and Avanzino; and (2) applicant's claims 8-15 may not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Yu in view of Hopper and Avanzino, and further in view of Chiang.

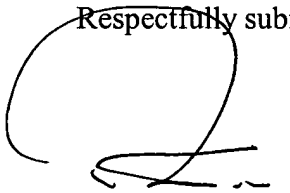
9. Summary

Applicant's invention as disclosed and claimed within claim 1 and claim 8 is directed at least in part towards a method for forming a dual damascene aperture through a dielectric layer. Applicant's method employs a patterned first dielectric layer and a blanket second dielectric layer formed of a corresponding first dielectric material and second dielectric material each having a dielectric constant of less than about 4.0, where the first dielectric material serves as an intrinsic etch stop with respect to the second dielectric material. A pertinent prior art reference employed in rejecting applicant's claims to applicant's invention may not properly be employed in rejecting applicant's claims to applicant's invention insofar as the pertinent prior art reference teaches away from that which is disclosed and claimed by applicant. Alternatively, absent from the pertinent prior art reference is: (1) a disclosure of each and every limitation within applicant's invention; and (2) a suggestion or motivation to modify or combine the prior art reference with other references since there is no likelihood of success upon such combination.

10. Conclusion

Applicant requests that the Board of Patent Appeals and Interferences reverse the Examiner's action in rejecting the claims within this application within the office action made FINAL. Allowance of all claims remaining within this application, in accord with the appended copy of the claims, is respectfully requested.

Respectfully submitted,



Randy W. Tung (Reg. No. 37,949)

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APPENDIX

COMPLETE COPY OF THE CLAIMS

1. A method for forming an aperture through a dielectric layer comprising:

providing a substrate;

forming upon the substrate a patterned first dielectric layer formed of a first dielectric material having a first dielectric constant of less than about 4.0, the patterned first dielectric layer defining a via;

forming upon the patterned first dielectric layer and filling the via a blanket second dielectric layer formed of a second dielectric material having a second dielectric constant of less than about 4.0;

forming over the blanket second dielectric layer a patterned mask layer which defines the location of a trench to be formed through the blanket second dielectric layer, where an areal dimension of the trench is greater than and at least in part overlapping an areal dimension of the via; and

etching, while employing the patterned mask layer in conjunction with an anisotropic etch method, the blanket second dielectric layer to form an aperture comprising:

the trench; and

at least a portion of the via, where the patterned first dielectric layer provides an intrinsic etch stop within the anisotropic etch method.

2. The method of claim 1 wherein the substrate is employed within a microelectronic fabrication selected from the group consisting of integrated circuit microelectronic fabrications, ceramic substrate microelectronic fabrications, solar cell optoelectronic microelectronic fabrications, sensor image array optoelectronic microelectronic fabrications and display image array optoelectronic microelectronic fabrications.

3. The method of claim 1 wherein the patterned first dielectric layer and the blanket second dielectric layer are each formed from a separate dielectric material selected from the group consisting of spin-on-polymer (SOP) dielectric materials, spin-on-glass (SOG) dielectric materials, amorphous carbon dielectric materials, diamond like carbon dielectric materials, carbonaceous silicate glass (CSG) dielectric materials, fluorosilicate glass (FSG) dielectric materials and aerogel dielectric materials.

4. The method of claim 1 wherein there is not formed an extrinsic hard mask layer interposed between the patterned first dielectric layer and the blanket second dielectric layer.

5. The method of claim 1 wherein the patterned first dielectric layer is formed to a thickness of from about 4000 to about 10000 angstroms.

6. The method of claim 1 wherein the blanket second dielectric layer is formed to a thickness of from about 4000 to about 7000 angstroms.

7. The method of claim 1 wherein the patterned mask layer is selected from the group consisting of patterned photoresist mask layers and patterned hard mask layers.

8. A method for forming a patterned conductor layer within an aperture through a dielectric layer comprising:

providing a substrate;

forming upon the substrate a patterned first dielectric layer formed of a first dielectric material having a first dielectric constant of less than about 4.0, the patterned first dielectric layer defining a via;

forming upon the patterned first dielectric layer and filling the via a blanket second dielectric layer formed of a second dielectric material having a second dielectric constant of less than about 4.0;

forming over the blanket second dielectric layer a patterned mask layer which defines the location of a trench to be formed through the blanket second dielectric layer, where an areal dimension of the trench is greater than and at least in part overlapping an areal dimension of the via;

etching, while employing the patterned mask layer in conjunction with an anisotropic etch method, the blanket second dielectric layer to form an aperture comprising:

the trench; and

at least a portion of the via, where the patterned first dielectric layer provides an intrinsic etch stop within the anisotropic etch method; and

forming within the aperture a contiguous patterned conductor interconnect and patterned conductor stud layer.

9. The method of claim 8 wherein the substrate is employed within a microelectronic fabrication selected from the group consisting of integrated circuit microelectronic fabrications, ceramic substrate microelectronic fabrications, solar cell optoelectronic microelectronic fabrications, sensor image array optoelectronic microelectronic fabrications and display image array optoelectronic microelectronic fabrications.

10. The method of claim 8 wherein the patterned first dielectric layer and the blanket second dielectric layer are each formed from a separate dielectric material selected from the group consisting of spin-on-polymer (SOP) dielectric materials, spin-on-glass (SOG) dielectric materials, amorphous carbon dielectric materials, diamond like carbon dielectric materials, carbonaceous silicate glass (CSG) dielectric materials, fluorosilicate glass (FSG) dielectric materials and aerogel dielectric materials.

11. The method of claim 8 wherein there is not formed an extrinsic hard mask layer interposed between the patterned first dielectric layer and the blanket second dielectric layer.

12. The method of claim 8 wherein the patterned first dielectric layer is formed to a thickness of from about 4000 to about 10000 angstroms.

13. The method of claim 8 wherein the blanket second dielectric layer is formed to a thickness of from about 4000 to about 7000 angstroms.

14. The method of claim 8 wherein the patterned mask layer is selected from the group consisting of patterned photoresist mask layers and patterned hard mask layers.

15. The method of claim 8 wherein the contiguous patterned conductor interconnect and patterned conductor stud layer is formed within the aperture while employing a chemical mechanical polish (CMP) planarizing method.